

This Page Is Inserted by IFW Operations  
and is not a part of the Official Record

## **BEST AVAILABLE IMAGES**

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

**IMAGES ARE BEST AVAILABLE COPY.**

**As rescanning documents *will not* correct images,  
please do not report the images to the  
Image Problem Mailbox.**

CLAIMS:

What is claimed is:

1 An interface for interconnecting electronic  
2 components, comprising:

3 at least one single-ended data signal;

4 a differential data signal pair;

5 a receiver for detecting said single-ended data  
6 signal, wherein detection of said single-ended data signal  
7 is made in conformity with a common mode voltage of said  
8 differential data signal pair.

1 2. The interface of Claim 1, wherein said receiver  
2 comprises:

3 a differential comparator coupled to said  
4 differential data signal pair; and

5 a singlential comparator coupled to said differential  
6 comparator and further coupled to said differential data  
7 signal pair and said single-ended data signal.

1 3. The interface of Claim 2, wherein said singlential  
2 comparator sums a non-inverted signal of said differential  
3 data signal pair and an inverted signal of said  
4 differential data signal pair to provide a reference for  
5 detecting said single-ended data signal.

SUB  
A1

09070623  
E2204860  
053104  
F01E50

1 4. The interface of Claim 2, wherein said singlential  
2 comparator comprises means for summing a non-inverted  
3 signal of said differential data signal pair and an  
4 inverted signal of said differential data signal pair to  
5 provide a reference for detecting said single-ended data  
6 signal.

1 5. The interface of Claim 3, wherein said singlential  
2 comparator comprises:

3 a first transistor having a gate coupled to said  
4 single-ended data signal ;

5 a second transistor having a gate coupled to a non-  
6 inverted signal of said differential data signal pair;

7 a third transistor having a gate coupled to an  
8 inverted signal of said differential data signal pair; and  
9

10 a current source coupled to a channel connection of  
11 said first transistor, a channel connection of said second  
12 transistor and a channel connection of said third  
13 transistor, whereby said singlential comparator detects a  
14 difference between said single-ended data signal and an  
15 average of said non-inverted signal and said inverted  
16 signal of said differential data signal pair.

1 6. The interface of Claim 5, wherein said differential  
2 comparator comprises:

3 a fourth transistor having a gate coupled to said  
4 non-inverted signal of said differential data signal pair;  
5 and

6 a fifth transistor having a gate coupled to said  
7 inverted signal of said differential data signal pair and  
8 a first channel connection coupled to a resistor for  
9 providing active mode operation; and

10 a current source coupled to a channel connection of  
11 said fourth transistor and a second channel connection of  
12 said fifth transistor, whereby said differential  
13 comparator detects a difference between said said non-  
14 inverted signal and said inverted signal of said  
15 differential data signal pair, and wherein a gain of said  
16 active mode of said differential comparator is equal to a  
17 a gain of said singlential comparator.

09870623 053101  
T01E00

1 7. The interface of Claim 2, wherein said receiver further  
2 comprises a multiplexer for producing a data output signal  
3 corresponding to said single-ended data signal, having a  
4 first input coupled to an output of said differential  
5 comparator, a second input coupled to an inverted output  
6 of said differential comparator, and a select input  
7 coupled to said output of said differential comparator and  
8 an output of said singlential comparator such that said  
9 output of said differential comparator is selected when  
10 said single-ended signal is at an equal logic value with  
11 said differential data signal pair and wherein said  
12 inverted output of said differential comparator is  
13 selected when said single-ended signal and said  
14 differential data signal pair are at unequal logic levels.

09870623-053101

1 8. The interface of Claim 7, wherein said receiver further  
2 comprises:

3 a first latch for coupling said differential  
4 comparator to said multiplexer, said first latch having an  
5 input coupled to said output of said differential  
6 comparator and an output coupled to said first input of  
7 said multiplexer;

8 an inverter having an input coupled to said output of  
9 said first latch for producing said inverted output of  
10 said differential comparator and having an output coupled  
11 to said multiplexer;

12 a second latch for latching said output of said  
13 singlential comparator; and

14 an exclusive-OR gate having a first input coupled to  
15 said output of said first latch and a second input coupled  
16 to an output of said second latch and an output coupled to  
17 a select input of said multiplexer for selecting said  
18 output of said first latch when said single-ended signal  
19 is at an equal logic value with said differential signal  
20 pair and for selecting said output of said inverter when  
21 said single-ended signal and said differential data signal  
22 pair are at unequal logic levels.

1 9. The interface of Claim 1, wherein said receiver  
2 comprises:

3 a first differential comparator coupled to said  
4 differential data signal pair;

5 a second differential comparator coupled to a non-  
6 inverted signal of said differential signal pair and said  
7 single ended-data signal;

8 a third differential comparator coupled to an  
9 inverted signal of said differential signal pair and said  
10 single ended data signal; and

11 means for selecting between an output of said second  
12 differential comparator and an output of said third  
13 differential comparator to produce a data output  
14 corresponding to a logic value of said single-ended data  
15 signal.

0987062345053101  
TOTAL

1 10. The interface of Claim 1, wherein said receiver  
2 comprises:

3 a first differential comparator coupled to said  
4 differential data signal pair;

5 a second differential comparator coupled to a non-  
6 inverted signal of said differential signal pair and said  
7 single ended-data signal;

8 a third differential comparator coupled to an  
9 inverted signal of said differential signal pair and said  
10 single ended data signal; and

11 a logic circuit coupled to said first differential  
12 comparator, said second differential comparator and said  
13 third differential comparator for selecting between an  
14 output of said second differential comparator and said  
15 third differential comparator to produce a data output  
16 corresponding to a logic value of said single-ended data  
17 signal.

09370523101



1 11. The interface of Claim 10, wherein said logic circuit  
2 comprises:

3 a multiplexer for producing said data output  
4 corresponding to said logic value of said single-ended  
5 data signal;

6  
7 a first latch having an input coupled to an output of  
8 said first differential comparator;

9 a second latch having an input coupled to an output  
10 of said second differential comparator and an output  
11 coupled to a first input of said multiplexer;

12 a third latch having an input coupled to an output of  
13 said third differential comparator and an output coupled  
14 to a second input of said multiplexer;

15 a first exclusive-OR gate having inputs coupled to  
16 said input of said first latch and said output of said  
17 first latch for detecting a difference between a present  
18 state and a prior state of said output of said first  
19 differential comparator;

20 a second exclusive-OR gate having inputs coupled to  
21 said input of said second latch and said output of said  
22 second latch for detecting a difference between a present  
23 state and a prior state of said output of said second  
24 differential comparator; and

25 a third exclusive-OR gate having inputs coupled to an  
26 output of said first exclusive-OR gate and an output of  
27 said second exclusive-OR gate, and having an output  
28 coupled to a select input of said multiplexer, for

29 performing said selecting.

1 12. The interface of Claim 11, further comprising a fourth  
2 exclusive-OR gate having inputs coupled to said input of  
3 said third latch and said output of said third latch for  
4 detecting a difference between a present state and a prior  
5 state of said output of said third differential  
6 comparator, and wherein said fourth exclusive-OR gate has  
7 an output coupled to an input of said third exclusive-OR  
8 gate.

09870623.053101  
TOTES0" E290/860

1 13. A receiver for receiving a differential data signal  
2 pair and a single-ended data signal, comprising:

3 a differential comparator coupled to said  
4 differential data signal pair; and

5 a singlential comparator coupled to said differential  
6 comparator and further coupled to said differential data  
7 signal pair and said single-ended data signal;

8 a multiplexer having an output for producing a data  
9 output signal corresponding to said single-ended data  
10 signal, having a first input coupled to an output of said  
11 differential comparator, a second input coupled to an  
12 inverted output of said differential comparator;

13 a first latch coupling said differential comparator  
14 to said multiplexer, said first latch having an input  
15 coupled to said output of said differential comparator and  
16 an output coupled to said first input of said multiplexer;

17 an inverter having an input coupled to said output of  
18 said first latch for producing said inverted output of  
19 said differential comparator and having an output coupled  
20 to said multiplexer;

21 a second latch for latching said output of said  
22 singlential comparator; and

23 an exclusive-OR gate having a first input coupled to  
24 said output of said first latch and a second input coupled  
25 to an output of said second latch and an output coupled to  
26 a select input of said multiplexer for selecting said  
27 output of said first latch when said single-ended signal

28 is at an equal logic value with said differential signal  
29 pair and for selecting said output of said inverter when  
30 said single-ended signal and said differential data signal  
31 pair are at unequal logic levels.

09870623-053101  
T0T50"E290/860

1 14. A receiver for receiving a differential data signal  
2 pair and a single-ended data signal, comprising:

3 a first differential comparator coupled to said  
4 differential data signal pair;

5 a second differential comparator coupled to a non-  
6 inverted signal of said differential signal pair and said  
7 single ended-data signal;

8 a third differential comparator coupled to an  
9 inverted signal of said differential signal pair and said  
10 single ended data signal;

11 a multiplexer for producing a data output  
12 corresponding to said logic value of said single-ended  
13 data signal;

14 a first latch having an input coupled to an output of  
15 said first differential comparator;

16 a second latch having an input coupled to an output  
17 of said second differential comparator and an output  
18 coupled to a first input of said multiplexer;

19 a third latch having an input coupled to an output of  
20 said third differential comparator and an output coupled  
21 to a second input of said multiplexer;

22 a first exclusive-OR gate having inputs coupled to  
23 said input of said first latch and said output of said  
24 first latch for detecting a difference between a present  
25 state and a prior state of said output of said first  
26 differential comparator;

27 a second exclusive-OR gate having inputs coupled to  
28 said input of said second latch and said output of said  
29 second latch for detecting a difference between a present  
30 state and a prior state of said output of said second  
31 differential comparator; and

32 a third exclusive-OR gate having inputs coupled to an  
33 output of said first exclusive-OR gate and an output of  
34 said second exclusive-OR gate, and having an output  
35 coupled to a select input of said multiplexer, for  
36 performing said selecting.

1 15. The receiver of Claim 14, further comprising a fourth  
2 exclusive-OR gate having inputs coupled to said input of  
3 said third latch and said output of said third latch for  
4 detecting a difference between a present state and a prior  
5 state of said output of said third differential  
6 comparator, and wherein said fourth exclusive-OR gate has  
7 an output coupled to an input of said third exclusive-OR  
8 gate.

09870623-053101

1  
2  
3

4  
56  
7

89

10  
11  
12  
13  
14  
15  
16

1 17. The comparator circuit of Claim 16, further  
2 comprising:

3 a fourth transistor having a gate coupled to said  
4 non-inverted signal of said differential signal pair; and

5 a fifth transistor having a gate coupled to said  
6 inverted signal of said differential signal pair and a  
7 first channel connection coupled to a resistor for  
8 providing active mode operation; and

9 a current source coupled to a channel connection of  
10 said fourth transistor and a second channel connection of  
11 said fifth transistor, whereby said differential  
12 comparator detects a difference between said said non-  
13 inverted signal and said inverted signal of said  
14 differential signal pair, and wherein a gain of said  
15 active mode of said differential comparator is equal to a  
16 a gain of said singlential comparator.

09870623-053101  
TOTED



1 18. A method for signaling over an electronic interface,  
2 said method comprising:

3     transmitting a differential data signal pair;  
4     second transmitting a single-ended data signal;  
5     receiving said differential data signal pair; and  
6     detecting said single-ended data signal in conformity  
7 with a common-mode voltage of said received differential  
8 data signal pair.

1 19. The method of Claim 18, wherein said detecting  
2 comprises:

3     deriving a reference from said differential pair of  
4 data signals; and

5     second detecting a difference between said single-  
6 ended data signal and said derived reference.  
7

1 20. The method of Claim 19, wherein said deriving is  
2 comprises summing currents proportional to a non-inverting  
3 signal of said differential data signal pair and an  
4 inverting signal of said differential data signal pair,  
5 and wherein said second detecting is comprises balancing a  
6 current proportional to said single ended data signal  
7 against said summed currents.

098706543210  
-053101  
T0T50

1 21. The method of Claim 18, wherein said detecting  
2 comprises:

3 first comparing a non-inverting signal of said  
4 differential pair to an inverting signal of said  
5 differential pair;

6 second comparing said single-ended data signal to  
7 said non-inverting signal of said differential data signal  
8 pair;

9 third comparing said single-ended data signal to said  
10 inverting signal of said differential data signal pair;  
11 and

12 selecting between a result of said second comparing  
13 and said third comparing, in conformity with a result of  
14 said first comparing and said second comparing.

1 22. The method of Claim 21, wherein said selecting is  
2 further performed in conformity with a result of said  
3 third comparing.

09870623-053101  
101